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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/978,018	10/17/2001	Hideki Takauchi	100021-00062	3806

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EXAMINER

NGUYEN, MINH T

ART UNIT PAPER NUMBER

2816

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

K-D

**Office Action Summary****Application No.**

09/978,018

**Applicant(s)**

TAKAUCHI ET AL.

**Examiner**

Minh Nguyen

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**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --****Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 December 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8, 10-17 and 19-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10-17 and 19-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 January 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/13/03 has been entered.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8, 10-17 and 19-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, the claim is rejected because the recited function on the last three lines does not have elements and/or structural to support (i.e., specific voltage levels and connections from the transmission line to the transistors, specific control voltage to the gates of the transistors, ..., are needed in order for the termination resistor circuit being able to perform the recited function). For further examination, it is assumed that the claim only requires a structure

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of the termination resistor circuit which is *capable of performing* the recited function since the structure to control the switching between the first and third transistors is not recited in the claim.

As per other independent claims, these claims are rejected for the same reasons noted in claim 1.

As per other dependent claims, these claims are rejected because of the indefiniteness of their independent claims.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-6, 8, 10-15, 17, 19-23 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,297,677, issued to Ang et al.

As per claim 1, Ang discloses a termination resistor circuit (Fig. 16), comprising:

a first termination resistor block (FETs 1610 and 1630) having a first diode connected transistor 1610 and a second not-diode connected second transistor 1630;

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a second terminal resistor block (FETs 1630 and 1620) having the second transistor 1630 and a third transistor 1620 which is not diode connected transistor;

the blocks are connected at terminals (drain and source, as shown) of the second transistor 1630; the recited limitation on the last four lines is merely the operation of the termination resistor circuit, since Ang has the same structure, the recited limitation is met.

As per claim 2, FETs 1610 and 1630 are both NFETs, and FET 1620 is PFET.

As per claim 3, Ang discloses a termination resistor circuit (Fig. 16), comprising:

a first termination resistor block (FETs 1610 and 1630), the gate of the first transistor 1630 being applied with a reference voltage VDD0 and the gate of the second transistor 1610 being *not* applied with the reference voltage VDD0 (as shown);

a second terminal resistor block (FETs 1610 and 1620) having the second transistor 1610 and a third transistor 1620 whose gate is *not* applied with the reference voltage ( $VSS \triangleleft VDD0$ );

the blocks are connected at terminals (drain and source, as shown) of the second transistor 1610; the recited limitation on the last four lines is merely the operation of the termination resistor circuit, since Ang has the same structure, the recited limitation is met.

As per claim 4, FETs 1610 and 1630 are both NFETs, and FET 1620 is PFET.

As per claim 5, rejected for the same reasons noted in claim 1.

As per claim 6, in column 15, lines 36-67, Ang teaches FETs having different sizes.

As per claim 8, rejected for the same reasons noted in claim 6.

As per claim 10, this claim is rejected for the same reasons noted in claim 1, and further, the limitations recited on the first five lines are explicitly disclosed in the Ang's abstract and shown in Fig. 1.

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As per claim 11, rejected for the same reasons noted in claim 2.

As per claims 12-13, rejected for the same reasons noted in claims 3-4, respectively, and further, the limitations recited on the first five lines are explicitly disclosed in the abstract and shown in Fig. 1.

As per claims 14-15 and 17, rejected for the same reasons noted in claims 5-6 and 8, respectively, and further, the limitations recited on the first five lines are explicitly disclosed in the abstract and shown in Fig. 1.

As per claims 19-20, rejected for the same reasons noted in claims 1-2, respectively, and further, the limitations recited on the first five lines are explicitly disclosed in the abstract and shown in Fig. 1.

As per claims 21-22, rejected for the same reasons noted in claims 3-4, respectively, and further, the limitations recited on the first five lines are explicitly disclosed in the abstract and shown in Fig. 1.

As per claim 23, rejected for the same reasons noted in claim 1, and further, the limitations recited on the first five lines are explicitly disclosed in the Ang's abstract.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,297,677, issued to Ang et al.

As per claim 7, Ang teaches the termination resistor circuit having FETs with different sizes as discussed in 6 but he does not explicitly disclose the FETs having the same sizes as called for in the claim.

However, the practice of varying the sizes of FETs to obtain the optimal and/or required condition for a certain applications is well within the level of one skilled in the art.

It would have been obvious to one skilled in the art at the time of the invention was made to use the first, second and third FETs in the Ang circuit having the same size. One skilled in the art would be motivated to do so when the application which uses the Ang circuit does not require a particular chosen weight.

As per claim 16, same as claim 7.

### ***Response to Arguments***

5. Regarding the argument Ang does not disclose the newly added limitation to each of the independent claims.

The examiner notes that due to the indefiniteness problem noted herein above, patentable weight is given to the newly added limitation only to the extent that if the reference has the recited structure, the functional recitation is met. In other words, because the Ang's termination resistor circuit has same structure, the Ang circuit is capable of performing the recited function.

Regarding the argument specific connections of the Ang's structure prevents the Ang's circuit from performing the recited function.

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The examiner notes that Ang teaches a termination resistor circuit for use with other circuit elements to perform other function by applying to the terminals of the transistors 1610, 1620 and 1630 different voltage signals as correctly identified by the applicants, however, the Ang's termination resistor circuit structure (comprises transistors 1610, 1620 and 1630) is still capable of performing the recited function, and therefore, the claimed circuit is still being anticipated by the Ang's structure. The word "comprising" used on line 2 of claim 1 does not exclude the other elements to be added to the termination resistor circuit for performing other function. In other words, Ang uses the termination resistor circuit having the same structure as the claimed termination resistor circuit for other purpose by adding other elements to the termination circuit, however, the Ang's termination resistor circuit structure alone (comprises transistors 1610, 1620 and 1630) is clearly capable of performing the function recited in the claim.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



2/3/04

Minh Nguyen  
Primary Examiner  
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